Key Value

- ✅ Accelerates UCIe chiplet development
- ✅ Automates layout-to-compliance workflow
- ✅ Reduces engineering effort and verification time
- ✅ Detects signal integrity issues early
- ✅ Minimizes costly package re-spins
- ✅ Supports UCIe-A and UCIe-S standards
- ✅ Integrates extraction, compliance, and simulation
- ✅ Generates executive-ready reports automatically
- ✅ Improves design confidence and first-pass success
- ✅ Enables faster time-to-market